REMARKS

The Examiner rejected claims 1, 3-6, 8, and 21-24 under 35 U.S.C. §103(a) as being unpatentable over by Zuraski, Jr. et al. (U.S. 6,260,134) in view of Nishi et al. (U.S. 5,918,045) in further view of Narayan et al. (U.S. 6,161,172).

Claims 1, 3-6, 8, and 21-24 are distinct over Zuraski, Nishii, or Narayan, whether taken alone or in combination, since the references neither disclose nor suggest at least "storing a plurality of instructions of different sizes in a plurality of buffer areas, each buffer area including a plurality of sub-buffers, each sub-buffer storing a unit instruction width, with an instruction of greater than a unit instruction width stored in more than one sub-buffer," as recited in amended claims 1 and 21.

The Examiner acknowledges that the combination of Zuraski and Nishi does not teach "using a plurality of buffers," but says that Nayaran teaches "receiving data containing instructions in a plurality of buffers" and identifies subqueues 86A-C of Nayaran's FIG. 4 as the plurality of buffers (sections 5 and 6 on page 4 of the office action). However, in section 7 on page 4 of the office action the Examiner inconsistently identifies the subqueues 86A-C of FIG. 4 as "a plurality of sub-buffers." Applicant contends that Nayaran, alone or in combination with the other references, does not teach "a plurality of buffer areas, each buffer area including a plurality of sub-buffers." Instead, Narayan describes:

> According to one embodiment, instruction identification information is shifted internally to each subqueue 86 independently. Instruction identification information is not, therefore, shifted from position I0 of subqueue 86B into positions within subqueue 86A. Instead, when each of the instructions within subqueue 86A have been dispatched, subqueue 86B is shifted into subqueue 86A as a whole. The logic for shifting between subqueues 86 may operate independently from and in parallel with the internal shifting of each subqueue 86A-86C. (column 19 line 65 – column 20 line 7)

Narayan's description of shifting "instruction identification information" between subqueues is neither equivalent to nor suggests outputting... from selected ones of the plurality of sub-buffers. Hence, Narayan does not suggest storing a plurality of instructions of different sizes in a plurality of buffer areas, each buffer area including a plurality of sub-buffers, each sub-buffer storing a unit instruction width, with an instruction of greater than a unit instruction width stored in more than one sub-buffer. Therefore, claims 1 and 21 are patentable over the referernces.

Dependent claims 3 and 23 further distinguish over the cited references by requiring "comparing a most significant bit of a [first] pointer ... to a most significant bit of a [second] pointer." The Examiner states that Nishii teaches this at column 8 lines 38-60. However, at column 8 lines 38-60 Nishii discloses receiving "enumerated values provided by the read pointer 510 and the write pointer 511." Nishii does not teach comparing any bits of the read pointer with any bits of the write pointer, much less "comparing a most significant bit" of one pointer with that of another, as required by claims 3 and 23.

Dependent claims 3-8 depend on claim 1, and dependent claims 23-24 depend on claim 21, and are therefore patentable for at least the same reasons as for claims 1 and 21.

The Examiner rejected claims 18-20 and 25-27 under 35 U.S.C. §103(a) as being unpatentable over Narayan in view of Nishi.

Claims 18-20 are distinct over these references since neither Narayan nor Nishi, alone or in combination, disclose or suggest "storing instructions of different widths within a cache having a plurality of buffer areas, each buffer area having a plurality of subportions, each subportion in the cache storing a unit instruction width, where ... an instruction of more than said unit width takes up more than one subportion within the cache," as recited in claim 25. Moreover the references also neither describe nor suggest "a plurality of buffer areas, each buffer area adapted to store a plurality of instructions of different widths in a plurality of subparts, each of said subparts storing a unit instruction width, and said instructions of greater than unit instruction width being stored in multiple said subparts," as recited in claim 27.

The Examiner states that Narayan teaches "a plurality of buffer areas [86A-C], adapted to store a plurality of instructions of different width in a plurality of subparts, each of said subparts storing a unit instruction width ..." in column 6 lines 23-65 (section 18 on page 6 of the office action). However, in column 6 lines 23-65, Narayan merely discloses "an instruction alignment unit 18" that includes "a byte queue configured to store instruction bytes." Even if, for the sake of argument, Narayan's "predefined number of instruction bytes" were interpreted as a "unit instruction width," nowhere does Narayan disclose or suggest "each buffer area having a plurality of subportions ... an instruction of more than said unit width takes up more than one subportion ..." Therefore, claims 25 and 27 are patentable.

As argued above for claims 3 and 23, claims 18 and 26 further distinguish over the cited references by requiring "comparing a most significant bit of a [first] pointer ... to a most significant bit of a [second] pointer."

Dependent claim 26 depends on claim 25, and dependent claims 18-20 depend on claim 27, and are therefore patentable for at least the same reasons as for claims 25 and 27.

Claim 22 has been cancelled. Applicants have also amended the claims to provide a clearer recitation of the inventions sought to be protected.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper.

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Respectfully submitted,

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